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| L11 same load | 3 |

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## Search History

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END OF SEARCH HISTORY

L9: Entry 1 of 2 File: USPT Feb 24, 2004

DOCUMENT-IDENTIFIER: US 6697275 B1
TITLE: Method and apparatus for content addressable memory test mode

Detailed Description Text (42):
In this example, the remaining two logic states derived from FIND_MATCH and FIND_MISS, `00` and `11`, may bring output signal PE to a `0` or `1` logic state, respectively. These latter test modes may be used to test various circuits that may follow a MUX 410 for defects by having inputs PE0 to PEy at a known data state (be it `0` or `1`). Such various circuits may include, but are not limited to, a match detection circuit, multiple match detection circuit, a priority encoder, or a ROM.

L4: Entry 1 of 9 File: USPT Jan 24, 2006

DOCUMENT-IDENTIFIER: US 6990001 B2
TITLE: Multiple match detection circuit and method

PRIOR-PUBLICATION:

| DOC-ID | DATE |
|---|---|
| US 20040130924 A1 | July 8, 2004 |

Brief Summary Text (2):
The present invention relates to content addressable memory. In particular, the present invention relates to a multiple match detection circuit for detecting a signal on a multiple matchline.

Brief Summary Text (8):
The circuit responsible for determining the existence of a match is the multiple match detection circuit. The multiple match detection circuit receives all the matchline sense circuit outputs as input signals after the search-and-compare operation, and determines one of two states. The first possible state represents the case where the search word does not match with any stored words or matches only one stored word. The second state occurs if the search word has matched with two or more stored words. The second state is significant because only one address of a matching word is returned as the resulting address of the search-and-compare operation. In such a case, if more than one match has resulted from the search-and-compare operation, there is at least one other stored word that matched the search word.

Brief Summary Text (9):
A prior art multiple match detection circuit and scheme is disclosed in commonly owned U.S. Pat. No. 6,307,798 titled Circuit and Method for Multiple Match Detection in Content Addressable Memory, filed Apr. 24, 2000, the contents of which are incorporated herein by reference. In the multiple match detection circuit of the prior art, a multiple matchline is precharged to a high voltage level, VDD for example, and subsequently discharged when there is at least one matchline sense circuit which outputs a signal indicating a match condition. There is one discharge transistor for each matchline sensing circuit output, and all discharge transistors are connected to the multiple matchline and in parallel with each other.

Brief Summary Text (10):
The multiple match detection circuit of the prior art compares the multiple matchline voltage level to a reference voltage during a sensing period in order to differentiate between the two different states. The reference voltage is fixed to mimic a multiple matchline having only one match, hence the multiple match detection circuit will sense if the multiple matchline voltage level is either above or below the reference voltage to generate the output corresponding to the first and second states respectively. The multiple match detection circuit therefore detects the discharged multiple match line to generate an output representing one of either the first and second states.

Brief Summary Text (11):
There are several disadvantages in the multiple match detection circuit and scheme

of the prior art. To reduce the silicon area occupied by the multiple match detection circuit, it is desirable to minimize the feature size of the discharge transistors. Since the current strength of a transistor changes directly with its feature size, the capacity of a small discharge transistor to pull a fully precharged matchline to ground is small. This results in very slow discharge of the multiple matchline, and increases the time required for the overall search and compare operation of the CAM. Inherent parasitic capacitance of the multiple matchline compounds this problem, which increases as CAM arrays store more words, and require more discharge transistors.

Brief Summary Text (12):
The optimal sensing margin for the multiple match detection circuit should be sufficient for the circuit to easily distinguish if the multiple matchline potential level is above or below the reference voltage. This optimal sensing margin is attained at the time when the multiple matchline voltage level has decreased to a potential level well below the reference voltage. Unfortunately, the poor voltage discharge rate of the multiple matchline previously described only allows accurate sensing to be performed at a relatively prolonged time after the multiple matchline voltage begins to fall.

Brief Summary Text (13):
The multiple match detection circuit and scheme of the prior art requires precise timing control between activation of the matchline sense circuits, activation of the reference voltage generator circuit and activation of the sense circuit within the multiple match detection circuit. Each above-mentioned circuit is activated in sequence according to specific, preset time delays, which are determined from the design parameters and simulations. Process variations during fabrication of the CAM chip and different operating conditions may cause slight shifts in the time delays, resulting in a false output from the multiple match detection circuit.

Brief Summary Text (14):
There is clearly a need for a mutliple match detection circuit capable of consuming very little power and detecting multiple matchline potential levels accurately at high speed.

Description Paragraph (19):
A typical CAM block diagram is shown in FIG. 1. The CAM 10 includes a matrix, or array 100, of CAM cells 101 arranged in rows and columns, where, for a ternary CAM, each cell stores one of three states: logic "1", logic "0" and "don't care", actually storing 2 bits of data. A predetermined number of CAM cells 101 in a row store a word of data. In the CAM array 100 of FIG. 1, there are n rows and m columns, where n and m are integer numbers. An address decoder 12 is used to select any row within the CAM array 100 to allow data to be written into or read out of the selected row although most commonly, data is written or loaded into the CAM and searched. The bidirectional data access circuitry 14 transfers data between the CAM array 100 and the data pins (not shown) of the CAM chip, for access by an external processor. Located adjacent to the CAM array 100 for each row is matchline sense circuitry block 200. Matchline sense circuitry block 200 comprises n matchline sense circuits and is used during search-and-compare operations for outputting an n-bit result 16 indicating a successful or unsuccessful match of a search word against the stored word. The matchline sense circuitry block results 16 for all rows are processed by the priority encoder 400 to output the address (Match Address) corresponding to the location of a matched word. Since it is possible that more than one row will match the search word, the priority encoder 400 generates the highest priority address corresponding to a matched word. Acting in parallel with the priority encoder 400 is a multiple match detection circuit 300, which assesses the matchline sense circuit results 16, and produces a two bit output Q1, Q0 representing the cases where there are no matches, only one match and two matches or more.

Description Paragraph (23):
FIG. 4 shows a multiple match detection circuit of the prior art. The circuit includes a multiple matchline MML, with many parallel connected discharge transistors 302 coupling MML to ground. The gate of each discharge transistor is connected to an output, ML.sub.--OUTi, of a matchline sense circuit 202. There is one discharge transistor 302 for each matchline sense circuit 202 output. The multiple matchline MML is connected to one input of a sense amplifier 310. A reference multiple matchline RMML is connected to another input of sense amplifier 310, having many parallel connected discharge transistors 306 coupling RMML to ground. Discharge transistors 306 are dummy discharge transistors, configured and sized identically to the discharge transistors 302, except that their gates are permanently grounded to keep them turned off. Only dummy discharge transistor 304 can be turned on by control signal MLSEN. The W/L ratio of dummy discharge transistor 304 is designed to be 1 1.5 times the size of the other normal and dummy discharge transistors 302 and 306 in order to distinguish between multiple match, single match or no match conditions. RMML has an equal number of dummy discharge transistors 304 and 306 as MML to ensure that voltage or temperature variations will affect MML and RMML equally, and that parasitic capacitance of both lines are matched. During operation, MLSEN turns on discharge transistor 304, and the voltage level of RMML will mimic the voltage level of MML when there is one match; ie, when one of ML.sub.--OUT0-ML.sub.--OUTm is at the high logic level.

Description Paragraph (25):
A description of the operation of the multiple match detection circuit of the prior art now follows with reference to FIGS. 3, 4 and 5. In the precharge state, all matchline sense circuits 202 (FIG. 3) are disabled, forcing ML.sub.--OUT0-ML.sub.--OUTm signals to the low logic level. Therefore, all discharge transistors 302 from FIG. 4 are turned off. Dummy discharge transistor 304 is also turned off since MLSEN is currently at the low logic level. With all discharge transistors turned off, MML and RMML FIGS. 4 and 5) are held at the high logic level by clamp transistors 311 and 321 respectively. Control signal SHL is at the low logic level, to disable the differential amplifier, and to reset outb and out to the high logic level via transistors 319 and 320. SHL.sub.--DLY and SHL.sub.--DLYb remain at the low and high logic levels respectively to keep transmission gate 326 turned off.

Description Paragraph (30):
The prior art circuit of FIG. 5 is subject to the previously mentioned disadvantages. The time required by the multiple match detection circuit 300 (FIG. 1) to sense the MML potential is lengthy. FIG. 6 is a plot of the multiple matchline voltage VMML as a function of time in the case where two or more discharge transistors 302 are turned on (in the multiple match condition). The multiple match detection circuit 300 (FIG. 1) compares VMML to a reference voltage VREF at a predetermined time, to sense if VMML is above or below VREF. Multiple match detection circuit 300 (FIG. 1) will generate a low logic level latch if VMML is above VREF, and a high logic level latch if VMML is below VREF. Sensing can be performed at time t1, but the sense margin is very small and a precise VREF voltage generator is required. A better sense margin can be achieved at later time t2 without the need for a high precision VREF voltage. The sensing margin for detecting between a multiple and single match case is only 0.5V which is subject to fluctuations due to process and temperature variations. However, the time between the start of VMML falling to t2 is wasteful because the CAM remains idle while waiting for the result of the comparison. Contributing to the prolonged sense time is the small feature size of discharge transistors 302 and 304 and 306. One conducting discharge transistor has a small current capacity, hence the discharge of MML (which begins in a high precharged state) to ground is very slow. Shrinking feature sizes will extend the optimal sense time past t2 because the discharge rate of VMML will be further diminished. To improve the sensing margin in the multiple matchline of the prior art, the width of dummy discharge transistor 304 is set from 1 1.5 times the size of discharge transistors 302 and 306. However, this size must be carefully selected, and the sensing margin remains relatively small.

Description Paragraph (32):
Sequential activation of the matchline sense circuits 200, the dummy discharge transistor 304 and the multiple match detection circuit is synchronised by the first, second and third predetermined times which are created from delay circuits. Since the start of the second predetermined time is dependent on the end of the first predetermined time, and the start of the third predetermined time is dependent on the end of the second, deviation in the duration of any predetermined time may result in the output of wrong data. As well, if the transient characteristics of the circuits change due to process variations, synchronisation can be lost.

Description Paragraph (33):
Reference will now be made to embodiments of the invention. Generally, the multiple matchline detection circuit of the present invention is a low power sense circuit for fast detection of no matches, a single match or multiple matches in the CAM cell array 100. This is achieved by setting a multiple matchline and a reference multiple matchline to a no-hit or miss default voltage level and pulling the multiple matchline to a hit voltage level before, at the same time, or after the reference multiple matchline is pulled to the hit voltage level. The multiple match detection circuit of the present invention employs a detecting circuit for detecting the first of the two multiple matchlines to reach the hit voltage level, and generates a two-bit output representing one of the states where 0, 1 or 2 and more stored words match the search word. The multiple matchline detection circuit is self-timed to disable sensing of the multiple matchline and reference multiple matchline.

Description Paragraph (35):
A more detailed schematic of the multiple matchline detection circuit is shown in FIG. 8 according to a first embodiment of the present invention. The configuration and connections of the discharge transistors 302 in relation to the multiple matchline MML is the same as described previously for the prior art multiple match detection circuit of FIG. 4. The configuration of the reference multiple matchline circuitry 333, and connections of the discharge transistors 306 in relation to the reference multiple matchline RMML is also the same as described previously for the prior art multiple match detection circuit of FIG. 4, with exception of transistor 305 which has its gate connected to the high voltage supply VDD. Since transistor 305 is no longer dependant on a timing signal, the reference circuit is self-timed. Also differing from the prior art is that transistor 305 is the same size as transistors 302 and 306, hence all discharge transistors 305 and 306 connected to RMML are constructed identically as discharge transistors 302 connected to MML to keep the parasitic capacitance of both multiple matchlines the same. MML and RMML are connected to their respective multiple matchline sense circuits 330 and 331, which receive as inputs, control signals EN1, EN2b and BIAS. The multiple matchline sense circuit 330 connected to MML will sense the voltage level of MML to generate signal MML.sub.--OUT, while the reference multiple matchline sense circuit 331 connected to RMML will sense the voltage level of RMML to generate signal RMML.sub.--OUT. A detecting circuit, implemented as a multiple match decoder 380, receives MML.sub.--OUT and RMML.sub.--OUT to generate a two bit, or multibit output Q1, Q0 and feedback control signal EN1.

Description Paragraph (45):
A description of the multiple matchline sensing operation in accordance with the present invention will now follow with reference to FIGS. 7, 13 and 14. It should be assumed that one or both of MML.sub.--OUT and RMML.sub.--OUT have been driven to the high logic level from the previous search-and-compare operation. The circuit of FIG. 13 will compare the rising voltage rate of the multiple matchline MML to a reference multiple matchline RMML, where the voltage level of MML will rise at a faster, slower or equal rate as the voltage level of RMML. The circuit will then output a two bit result representing one of the three states of MML. After the

matchline sense circuits 210 (FIG. 7) have completed their comparison of the search word against their respective stored words, none, one or more ML.sub.--OUTi (MLOUT0-ML.sub.--OUTn) signals will be driven to the high logic level to indicate the occurrence of a match. Hence, any logic high ML.sub.--OUTi will immediately turn on its respective discharge transistor 302 from the multiple match detection circuit of FIG. 13. This will have no effect on MML because the multiple match sense circuit 330 is in the precharge phase in which the current source 332 is turned off and precharge transistor 354 is turned on via signal EN1 at the high logic level to hold MML to low logic level. The multiple match sense circuit 331 connected to RMML is also in the precharge phase due to the high logic level of EN1. Current is then applied to the multiple matchline MML and the reference multiple matchline RMML during the sensing phase when EN1 is set to the low logic level. OR gate 382 generates a low logic level EN1 signal as long as both MML.sub.--OUT and RMML.sub.--OUT remain at the low logic level. This will occur when EN2b pulses high at the input to NOR gate 362 of multiple match sense circuit 330 and at the input to NOR gate 362 of multiple match sense circuit 331 to start the active phase. The low logic levels of MML.sub.--OUT and RMML.sub.--OUT are latched via feedback inverters 360, and will remain so until either one of MML and RMML rises to the threshold voltage of its respective sense transistor 342 during the search-and-compare operation. In the case of no matches, no current path is formed between MML and ground, thus allowing the voltage of MML to rise quickly over time. In the case of a single match, where one current path is formed between MML and ground through a single discharge transistor 302, the rate at which the voltage of MML rises over time is slower because a small amount of charge is continually discharged from the multiple matchline MML by the single current path to ground. Therefore the rising rate of the multiple matchline MML voltage over time in the case of a single match is slower than the rising rate in the case where there are no matches. This rising rate becomes even slower due to the existence of multiple parallel current paths between the multiple matchline MML and ground in the case where two or more discharge transistors are turned on, since the current source 332 must overcome multiple pull down paths. The voltage level of RMML will rise at a rate consistent with MML having exactly one discharge transistor 302 turned on. In the present embodiment, only the gate of one discharge transistor 305 is connected to VDD, and the remaining discharge transistors 306 connected to RMML have their gates connected to ground. Therefore the voltage level of RMML will always rise at a rate corresponding to the single match condition.

Description Paragraph (51):
First transition arrow 500 indicates the beginning of the EN2b precharge pulse which simultaneously drives and latches MML.sub.--OUT and RMML.sub.--OUT to the low logic level. Accordingly, D1 and D0 follow the logic levels of MML.sub.--OUT and RMML.sub.--OUT respectively as indicated by second and third transition arrows 502 and 504. When both MML.sub.--OUT and RMML OUT are at the low logic level, OR gate 382 generates a low logic level EN1 to turn on current sources 332 from multiple match sense circuits 330 and 331, as shown by fourth and fifth transition arrows 506 and 508. EN1 at the low logic level will end the precharge phase and start the sense phase as shown by sixth transition arrow 510. By enabling the current sources 332 of the multiple matchline sense circuit 330 and reference multiple matchline sense circuit 331, the voltage levels of MML and RMML will begin to rise. The voltage level of MML will reach the Vt voltage to turn on sense transistor 342 of multiple matchline sense circuit 330 before the voltage level of RMML reaches the Vt voltage level. At seventh transition arrow 512, MML.sub.--OUT is subsequently latched at the high logic level. The high logic level of MML.sub.--OUT is reflected in the transition of D1 to the high logic level. At this time, outputs Q0 and Q1 follow the D0 and D1 logic levels. Because RMML has not reached the voltage of Vt, RMML.sub.--OUT will remain at the precharged low logic level. The high logic level of MML.sub.--OUT will cause OR gate 382 to drive EN1 to the high logic level at the eighth transition arrow 514. Two events occur simultaneously as a result of EN1 being driven to the high logic level. First, at ninth transition arrow 518, DFF 384 and 385 latch their respective D inputs (D1 and D0) from signals MML.sub.--OUT and

RMML.sub.--OUT in response to the transition of EN1 to the high logic level. Since Q0 and Q1 have latched the low and high logic levels respectively, any further changes to the logic levels of MML.sub.--OUT and RMML.sub.--OUT will have no effect on Q0 and Q1. Note according to Table 2 above, the high logic level Q1 and the low logic level Q0 represents the no match output state of the multiple match detection circuit, which correctly corresponds to this situation in which all ML.sub.--OUTi signals are at the low logic level. This is an advantageous feature of the present invention because RMML.sub.--OUT changes to the high logic level shortly after MML.sub.--OUT when RMML reaches the Vt voltage level, but is prevented from changing Q0 to the high logic level and changing the output state of the multiple match detection circuit. The second event caused by EN1 takes place at transition arrow 520. EN1 will turn off all current sources 332 via transistor 350, and turn on all precharge transistors 354 to quickly pull down multiple matchlines MML and RMML to ground. The multiple matchline sense circuits 330 and 331 are now reset to the precharge phase and ready to perform another sense operation.

CLAIMS:

4. The multiple match detection circuit of claim 1, wherein multiple discharge transistors are coupled in parallel between the sense line and ground, the gate of each of the multiple discharge transistors being coupled to an output from a respective matchline sense circuit.

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L12: Entry 1 of 3 File: USPT Sep 12, 1978

DOCUMENT-IDENTIFIER: US 4114010 A
TITLE: Test circuit and method for matching an induction load to a solid state power supply

Brief Summary Text (6):
The load circuit for induction heating equipment often includes a variable ratio transformer having a primary winding connected to the power source and a secondary winding connected to the inductor. In connection with such a variable ratio transformer arrangement, the test circuit of the present invention advantageously enables obtaining an impedance match in the load circuit as well as a frequency match between the load circuit and power supply. In this respect, for any given number of power factor correction capacitors in a load circuit there is a voltage known to be indicative of optimum impedance balance. Therefore, the voltmeter connected across the output of the audio frequency oscillator can be calibrated to give an indication of a voltage reading corresponding to an optimum impedance match for a given number of capacitors. Then, by varying the transformer ratio, various voltage readings are obtained for comparison with the voltage indicated for optimum impedance matching. The transformer ratio providing the voltage closest to the calibrated voltage is the transformer ratio which will provide the best impedance match for the number of capacitors which are in the load circuit following the frequency matching operation.

Detailed Description Text (9):
In addition to matching the frequency of the load circuit and power supply as described hereinabove, it is desirable to provide an impedance match in the load circuit. In the embodiment shown this capability is present as a result of the variable ratio winding transformer, and test circuit C advantageously enables obtaining the most desirable impedance match once the frequency match has been made. In this respect, as graphically illustrated in FIG. 3, the taps on primary winding 80 of transformer T can be changed and, in response thereto, for example, voltages V.sub.1, V.sub.2 and V.sub.3 will be observed from voltmeter 98. The voltmeter can be appropriately calibrated to indicate a voltage V corresponding to the optimum impedance match for the number of capacitors in the circuit as a result of the frequency matching operation. By comparing voltages V.sub.1, V.sub.2 and V.sub.3 with voltage V, the turn ratio providing the most desirable impedance match can readily be determined.

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